Thesis Summary

In wireless communication systems, the local oscillator (LO) plays an important role. The oscillator used in a RF transceiver is usually embedded in a phase-locked loop (PLL) system so as to achieve a stable and precise definition of the output frequency, and this system is called “frequency synthesizer”. Synthesizer design still remains one of the most challenging issues in RF systems because it must meet very stringent requirements such as: settling time, phase noise, reference spur, etc. To reach an appropriate compromise among these requirements, we have proposed a new architecture adopting the high-resolution phase error calibration circuits and automatic frequency control (AFC) circuits to achieve a fast locking, wide range, and low reference spur PLL.

To satisfy the IEEE 802.11a WLAN standards in the 5 GHz bands, a dual-band PLL-based frequency synthesizer is designed and fabricated in TSMC 0.18-μm CMOS technology. The chip size is 0.92 mm $\times$ 0.83 mm. At 5.76 GHz, the measured output spur level is less than -63 dBc after the high-resolution phase error calibration circuits are active. Throughout the whole output frequency range, the measured reference spurs are suppressed by 5.6-6.7 dB with calibration. The synthesizer draws 16 mA from a 1.8-V power supply, and the measured phase noise is -104 dBc/Hz at an offset frequency of 1 MHz.

Index Terms—Phase error calibration, high-resolution phase detector (HRPD), spur suppression, frequency synthesizer